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ABSTRACT OF THE DISCLOSURE

A semiconductor device having a plurality of wiring layers in a multi-layered structure, includes an inner area at a surface and a pad area surrounding the inner area therein, and further includes a device fabricated below the pad area. The device is comprised of at least one of a bypass capacitor, a protection device, and an input/output device. For instance, the bypass capacitor is comprised of metal wire layers arranged below the pad area.